Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (currently amended): An integrated circuit comprising:

at least three cooperating frequency domains having variable operating frequencies, wherein the at least three domains each operate at different frequencies;

cross-over logic to allow integral fractional ration frequency domain cross-overs between more than one pair of frequency domains; and

a mask generator circuit to compute and generate masking signals for said cross-over logic on the fly using selectable cross-over ratios.

Claim 2 (original): The integrated circuit of claim 1 wherein said cross-over logic is capable of providing at least sixteen different cross-over ratios.

Claim 3 (original): The integrated circuit of claim 1 wherein said at least three cooperating frequency domains comprise:

a processor domain operable at a relatively large number of different frequencies;

a memory control domain;

a memory interface domain operable at a first relatively small number of frequencies, said first relatively small number being less than one-half of the relatively large number;

a bus interface domain operable at a second relatively small number of frequencies, said second relatively small number also being less than one-half the relatively large number.

Claims 4-11 (canceled)

Claim 12 (currently amended): A system comprising:

an integrated circuit comprising:

a CPU portion to operate at a selectable first frequency which is one of a first plurality of frequencies, said first plurality of frequencies being equal to a base frequency plus between zero and N times an incremental frequency;

a graphics portion to operate at a second frequency which is a function of the selectable first frequency;

a memory control portion to operate at said second frequency;

a memory interface portion to operate at a third frequency;

a bus interface portion to operate at a fourth frequency;

programmable cross-over logic to interface said bus interface portion and said memory interface portion to said memory control portion at selectable integral fractional clocking ratios;

a memory subsystem to communicate with said memory interface portion, wherein each portion operates at a different frequency; and

mask generation circuitry to compute and generate mask signals for said programmable cross-over logic.

Claims 13-21 (canceled)

Claim 22 (currently amended): An integrated circuit comprising:

a first portion operable at a first plurality of frequencies, said first portion to operate in a first frequency domain;

a second portion operable at a second plurality of frequencies that are a ratio n/m to said first portion, said second portion to operate in a second frequency domain;

cross-over logic between said first portion and said second portion, said cross-over logic comprising:

a plurality of latches arranged as a FIFO array;

a plurality of status bits comprising:

a plurality of free bits;

a plurality of valid bits;

a writer element to maintain a write pointer to said FIFO array in said first frequency domain;

a reader element to maintain a read pointer to said FIFO array in said second frequency domain;

domain crossing handshake circuitry to update said plurality of free bits and said plurality of valid bits;

a third portion operable at a third plurality of frequencies, said third portion to operate in a third frequency domain, wherein the first, second and third portions each operate at different frequencies; and

mask generation circuitry to compute and generate mask signals for said cross-over logic.

Claim 23 (previously presented): The integrated circuit of claim 22 wherein said domain crossing handshake circuitry comprises:

writer assertion logic to toggle a writer indicator signal to either a first or a second logic value to indicate available write data;

reader response logic to receive said writer indicator signal and to indicate that valid data is available responsive to the writer indicator signal toggling to either the first or the second logic value;

reader assertion logic to toggle a reader indicator signal to either the first or the second logic value to indicate that a data item has been used;

writer response logic to receive said reader indicator signal and to indicate that a free FIFO entry is available responsive to the reader indicator signal toggling to either the first or the second logic value.

Claims 24-29 (canceled)